Roll No. : .....

MEERUT INSTITUTE OF ENGINEERING AND TECHNOLOGY

NH-58, Delhi-Roorkee Highway, Baghpat Road, Meerut – 250 005 U.P.

Pre University Test (PUT) : Odd Semester 2022-23

Course/Branch : **B Tech - CSE and Allied Branches** | **Semester** : **III**
Subject Name : **Computer Organization and Architecture** | **Max. Marks** : **100**
Subject Code : **(KCS302)** | **Time** : **180 min**

CO-1 : Illustrate and interpret the basic structure, operation of the computer system and apply the basic concepts to its components. (K1, K2, K3)

CO-2 : To Apply the basic logic for arithmetic & logic unit design and summarize the floating & fixed points arithmetic operations. (K2, K3)

CO-3 : To Understand the control unit techniques & micro programming controls and compute different pipeline techniques. (K3)

CO-4 : To Understand the hierarchical memory systems and correlate the cache and virtual memory. (K2, K4)

CO-5 : Illustrate the diversity of communication to I/O devices with peripherals and interrupts. (K2, K4)

Section – A # 20 Marks (Short Answer Type Questions)

Attempt **ALL** the questions. Each Question is of 2 marks (10 x 2 = 20 marks)

Q. No.		COx	Question Description # Attempt **ALL** the questions. Each Question is of 2 marks	
1	A	CO1	What are different types of Buses? Explain each one in brief.	K2
	B	CO1	Define addressing modes. What are its types? Explain each type using suitable example	K2
	C	CO2	Draw flow chart for division operation	K2
	D	CO2	Draw and explain Look ahead carry adder.	K2
	E	CO3	Define instruction Format and its type.	K2
	F	CO3	Explain instruction pipeline	K2
	G	CO4	Define SRAM and DRAM.	K2
	H	CO4	What do you mean by Virtual memory ?	K2
	I	CO5	Define hardware interrupts. What are its types?	K2
	J	CO5	What do you mean by I/O interface?	K2

Section – B # 30 Marks (Long / Medium Answer Type Questions)

Attempt **ALL** the questions. Each Question is of 6 marks (5 x 6 = 30 marks)

Q No2	CO1	What is stack ? Give the organization of register stack with all necessary elements and explain the working of push and pop operations. Or Discuss the advantages and disadvantages of polling and daisy chaining bus arbitration schemes.	K2 K2
Q No 3	CO2	Perform the division process of 00001111 by 0011 (use a dividend of 8 bits). Or Draw the flowchart of Booth's algorithm for multiplication and show the multiplication process using Booth's algorithm for (– 7) × (+ 3).	K3 K3
Q No 4	CO3	Differentiate between Hardwired and Micro programmed control Units? Or What do you means by Program control and list its types	K2 K2
Q No 5	CO4	What are the different Cache mapping Techniques Or The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words each. Physical memory consists of 4K blocks of 4K words each. Formulate the logical and physical address formats.	K2 K3
Q No 6	CO5	Differentiate between Vectored and Non vectored Interrupt Or Draw and explain CPU-IOP communication	K2 K2

Section – C # 50 Marks (Medium / Long Answer Type Questions)

Attempt ALL the questions. Each Question is of 10 marks.

Q.7 (CO-1) : Attempt any TWO question.

a)Draw and explain in detail General Register Organization. **K2**

b) What do you understand by CPU Organization. **K2**

c) A digital computer has a common bus system for 8 registers of 16 bit each. The bus is constructed using multiplexers. **K3**

I. How many select input are there in each multiplexer?

II. What is the size of multiplexers needed? III. How many multiplexers are there in the bus?

Q.8 (CO-2) : Attempt any ONE question.

a) Explain IEEE standard for floating point numbers and Represent $(1460.12510)_{10}$ in single precision and double precision formats. **K2**

b. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 5-bit registers that hold signed numbers. The multiplicand in both cases is + 15. **K3**

I. (+15) x (+13)

II. (+15) X (-13)

Q.9 (CO-3) : Attempt any ONE question.

a) Draw and Explain Instruction cycle Flow chart in detail. **K2**

b) Differentiate between horizontal and vertical Micro programming. **K2**

Q.10 (CO-4) : Attempt any ONE question.

a. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R 1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register. **(K4)**

b. What do you understand by Main Memory Also explain DRAM and SRAM in detail **K2**

Q.11 (CO-5) : Attempt any ONE question. .

a. What are the different modes of data transfer? Explain each one in detail. **K2**

b. Define Synchronous and Asynchronous communication detail with necessary timing diagrams. **K2**